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3-6-03
J. Garner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Lin et al.	Art Unit:	2814
Serial No.:	09/975,444	Examiner:	Pham, L.
Filing Date:	10/11/2001	Docket No.:	TI-31518
Title:	ELIMINATION OF OVERHANG IN LINER/BARRIER/ SEED LAYERS USING POST-DEPOSITION SPUTTER ETCH		

Amendment under 37 CFR 1.111

Assistant Commissioner of Patents
Washington, DC 20231

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 11/04/2002. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Replace claim 1 with the following claim:

1. (amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a dielectric layer over a semiconductor body;

forming a hole in said dielectric layer;

depositing a metal layer over said dielectric layer including in said hole using physical vapor deposition;

performing a sputter etch using a low bias after said step of depositing the metal layer; and

then, depositing a metal filler to fill said hole.

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